A DISTRIBUTED BROADBAND MONOLITHIC FREQUENCY MULTIPLIER

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ABSTRACT

A broadband frequency doubler, which employs distributed amplifier techniques, has been designed to operate over several octaves of bandwidth. The new circuit design suppresses the fundamental frequency energy present at the output port while maximizing the second harmonic signal. The design can be realized using monolithic or conventional microwave circuit techniques for use in local oscillator chains.

INTRODUCTION

Frequency multipliers are used in a variety of applications to extend the upper frequency limit of fixed or variable frequency oscillators. However, as the bandwidth of the multiplier approaches an octave, simple circuits become less useful because of the fundamental frequency energy which is present at the multiplier's output port. This problem is typically overcome by using a balanced structure to suppress the fundamental frequency, such as a transformer or microstrip balun which also have bandwidth constraints.

The proposed frequency multiplier employs distributed amplifier techniques to synthesize a circuit configuration with inherent broadband and balanced characteristics. The proposed circuit (Figure 1) employs a common input network which forms a lumped-element transmission lines of impedance Z_o. The output circuit is composed of two lumped-element transmission lines of impedance $2Z_o$. The number of active/passive element circuit sections are arbitrary and are chosen to meet specific gain, bandwidth, and power output requirements.

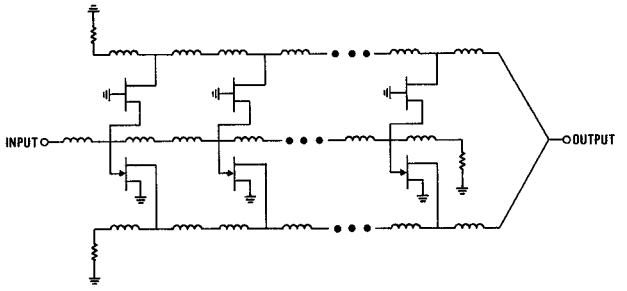

Figure 1. Distributed Balanced Multiplier Concept

DESIGN

In order to demonstrate the multiplier concept, a two cell monolithic circuit was designed. The doubler is composed of four FETs with gate widths of 176 μm. As depicted in Figure 2, two FETs are connected in a common gate configuration while the other two devices are connected in a common source configuration. Since the input voltage at either the input source or gate of each section is applied at a common node, the output voltage present on each drain transmission line output node can be made anti-phasal. The amplitudes of each signal can also be made equal by proper circuit element selection. However, although there is an inherent 180 degrees of phase shift between common gate and common source configurations at the fundamental frequency, the phase shift at the second harmonic is 360 degrees. Thus, if the output of each side of the circuit is summed at a common node, the fundamental signal will be cancelled and the second harmonic will be maximized. This condition can occur over a significant bandwidth which is typically greater than a decade

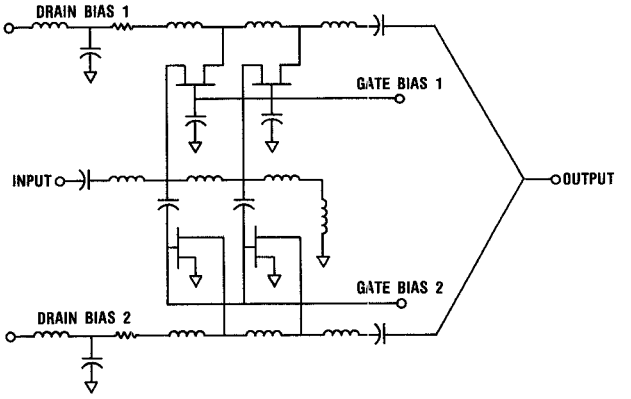

Figure 2. Frequency Multiplier Schematic Illustrating DC Bias Arrangement

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wide. The second harmonic of the circuit is also maximized by optimizing the FET bias point (Figure 3). This suppression of the fundamental input signal present at the circuit output for the multiplier chip (Figure 4), which is a measure of the circuit balance, is

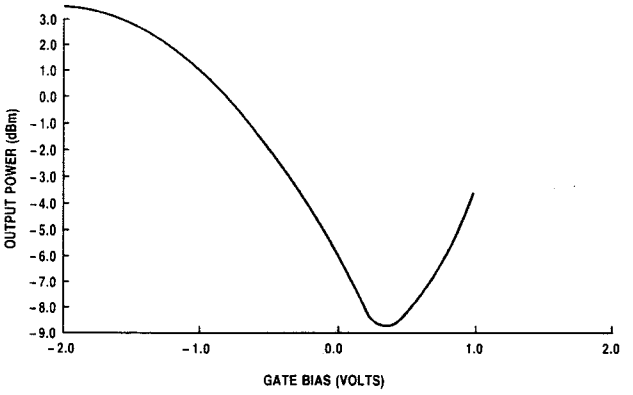

Figure 3. Second Harmonic Output Power as a Function of Gate Bias for a Typical 300μm FET

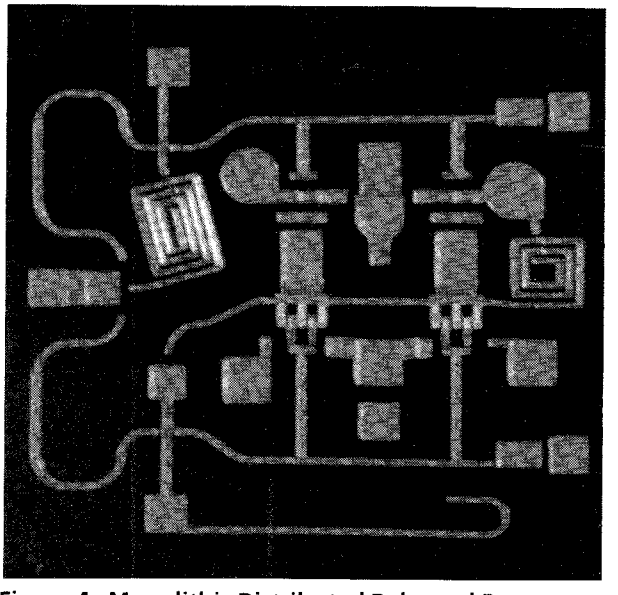

Figure 4. Monolithic Distributed Balanced Frequency Multiplier Chip

shown in Figure 5. The second harmonic output power, as a function of drive power, is also illustrated in Figure 5.

MODULE PERFORMANCE

The completed frequency doubler chip was used in the design of a 5 to 9 GHz (10 to 18 GHz output frequency) multiplier chain (Figure 6). The chain employed several stages of post and preamplification to set input drive levels and to provide increased LO power. With the balanced multiplier biased for maximum second harmonic output, the power output of the chain was evaluated as a function of drive power. The data, which includes the harmonic output power and the fundamental feed-through power

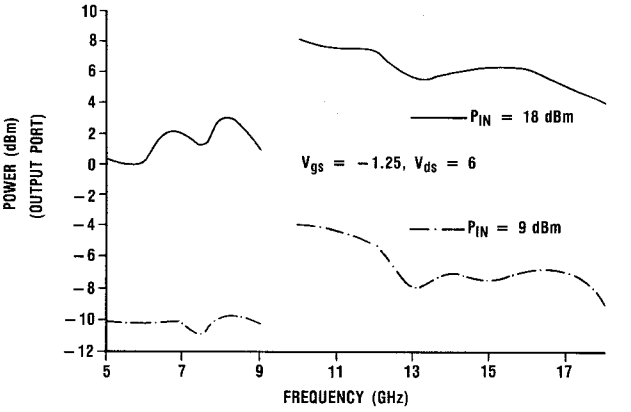

Figure 5. Power Output and Fundamental Suppression of Multiplier Chip

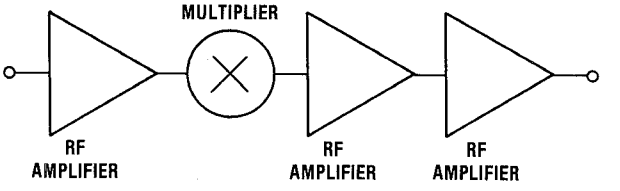

Figure 6. Block Diagram of Frequency Multiplier Chain

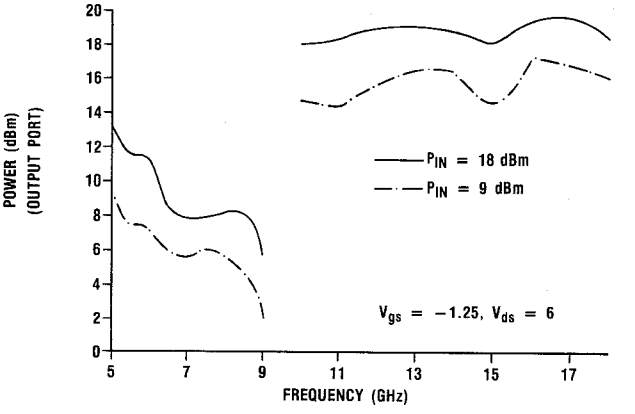

Figure 7. Power Output Performance of Multiplier Chain

present at the output port, is illustrated in Figure 7. As can be seen, a 9 dB variation in input power produces only 3 db of output power variation. With the chain fully driven, the total power output variation is less than +/- 1 dB, which is considerably better than most wide band oscillators.

CONCLUSION

This synthesis approach can be employed in the design of a variety of frequency multiplier circuits which will greatly reduce the complexity of conventional local oscillators chains commonly in use. The multipliers exhibit excellent power output characteristics, with fundamental frequency suppression, and require no tuning, which is certainly not the case with diode multipliers.